IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of: Examiner: Jennifer M. Dolan

Knall et al.

Serial No. 10/689,187 Group Art Unit: 2813

Filed: October 20, 2003 Docket No: SAND-01136US0

(formerly MA-002-1-I-a)

For: Three-Dimensional Memory Array and Method of Fabrication

REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 29, 2007

To the Commissioner:

An Appeal Brief was filed in the above-captioned case on December 22, 2006. Appellant respectfully files this Reply Brief in response to the Examiner's Answer mailed on March 29, 2007. An Appendix listing the pending claims is included in this Reply Brief.

SUMMARY

The following discussion responds to the Examiner's Answer mailed March 29, 2007. Rebuttal is made to points raised by the Examiner in her Response to Argument, beginning at paragraph 10 on page 8. In the interest of brevity, Appellant has tried to limit rebuttal to new points raised in the Examiner's Answer. Where Appellant believes the Examiner's arguments to have been sufficiently addressed by the Appeal Brief, those arguments will be allowed to stand and will not be repeated.

DISCUSSION

This Discussion will identify points in the Response to Argument section of the Examiner's Answer that require rebuttal, then will provide such rebuttal.

- **Page 8, paragraph beginning "In response, the Examiner ..."**

The Examiner concedes Appellant's argument that the use of amorphous silicon or silicon nitride as an antifuse material will only eliminate switch-off phenomena when accompanied by the low thermal resistance conductors of Zhang '302, which was the Examiner's suggested motivation to combine the reference. The Examiner then maintains that because the appealed claims do not specifically recite these low thermal resistance materials or elimination of switch-off, the point is moot.

Appellant will respectfully note that to rebut a rejection under 35 USC 103(a), Appellant's responsibility is to explain why one skilled in the art would not be motivated to make the combination suggested by the Examiner. Appellant has done so, and the Examiner has conceded Appellant's argument. Whether or not the claims refer to elements in the references used by the Examiner has no bearing on this determination; in fact the less relevant the references selected by the Examiner, the less likely that the claims will in fact refer to such elements.

- **Page 9, paragraph beginning "In response to these arguments ..."**

The Examiner responds to Appellant's argument:

> ... It is noted that despite the Appellant's argument that figures 5a-6e in Zhang '396 teach an MPROM embodiment that does not include an antifuse, Zhang '396 specifically identifies quasi-conduction layer '502 as a thin amorphous silicon layer or ceramic oxide layer ... and later states that

> thin amorphous silicon layers or ceramic oxide layers function as antifuses … Thus, the Examiner maintains that Zhang '396 and '302 are considered to have similar materials and similar structures, and thus be reasonably combined.

Appellant concedes that this point was made very briefly in the Appeal Brief, and appreciates the opportunity to provide more detail. Figures 6b-6e, used by the Examiner, refer to MPROM (Zhang '369, col. 2, lines 63-64).

Appellant points out that MPROM is mask-programmed read-only memory. MPROM is a well-known term of art (though the term "mask ROM" or MROM" is more widely used.) A typical definition appears at www.wikipedia.com:

> One of the earliest forms of non-volatile read-only memory, the mask-programmed ROM was prewired at the design stage to contain specific data; once the mask was used to manufacture the integrated circuits, the data was cast in stone (or at least in silicon) and could not be changed. Whatever 1's and 0's were in memory when it left the factory were there for life.

An explanation of the two types of ROM appears in Zhang '396 at col. 1, lines 23-28:

> ROM can be categorized into two classes: mask programmable ROM (MPROM), and electrically programmable ROM (EPROM). In MPROM, digital information is defined by masks during manufacturing, while in EPROM, information can be configured by end users.

The memory state of MPROM is programmed into the memory *during fabrication*, and cannot be changed by the end user. This is in contrast to field-programmable memory such as EPROM, in which all memory cells are fabricated unprogrammed, and individual cells in the memory are programmed by the end user.

The purpose of the antifuse in the EPROM embodiments of Zhang '396 is to store the memory state of the cell. When the antifuse is in its original, unprogrammed state, the value of the cell is, for example, a '0'. After the antifuse is ruptured during programming of the cell by the user, the value of the cell is, for example, a '1'.

In MPROM, however, no such change takes place. Each memory cell is fabricated as a '0' or a '1', and *never changes state*. An antifuse, by definition, changes state from insulating to conductive. Since there is no change in memory state in any memory cell in an MPROM array, logically there cannot be any element in a MPROM cell behaving as an antifuse, no matter what materials are used to form it. A layer such as the Examiner describes may exist in this cell, but, since it is an MPROM cell, clearly there can be no intention to rupture this layer. Thus any teaching on how to form a memory cell in an

MPROM array can have no relevance to one skilled in the art selecting material to use for an antifuse.

Appellant believes the remainder of the Examiner's arguments have largely been addressed in the Appeal Brief and thus will not repeat them here.

CONCLUSION

Appellant respectfully solicits the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

May 29, 2007
Date

/Pamela J. Squyres/
Pamela J. Squyres
Reg. No. 52,246

Vierra Magen Marcus & DeNiro LLP
575 Market Street, Suite 2500
San Francisco, CA 94105-2871
Telephone: (415) 369-9660 x215
Facsimile: (415) 369-9665

APPENDIX

The following claims are under appeal:

1. A three dimensional multi-level memory array disposed above a substrate, the array comprising:
   a first plurality of spaced-apart rail-stacks disposed at a first height in a first direction above the substrate;
   a second plurality of spaced-apart rail-stacks disposed above the first height and in a second direction different from the first direction; and
   a plurality of memory cells, each memory cell comprising a silicon nitride antifuse,
   wherein the antifuses are disposed at the intersections of the first rail-stacks and the second rail-stacks.

2. The array of claim 1, further comprising polysilicon p+n- diodes or polysilicon p-n+ diodes.